SiW Electromagnetic Calorimeter - The EUDET Module

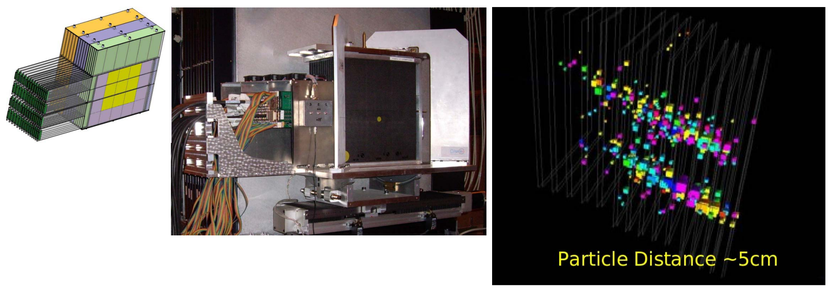
Calorimeter R&D for the ILC within the CALICE collaboration

The groups working on the EUDET Electromagnetic Calorimeter

This project is partially funded by the European Union in the 6th Framework Program "Structuring the European Research Area"

Physics Prototype

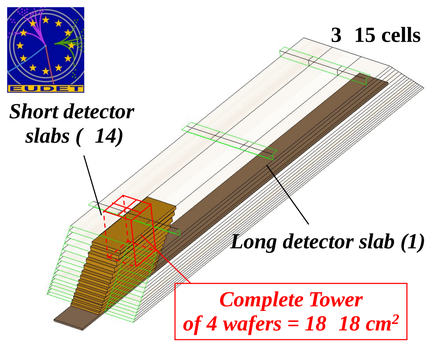
Validating concept of highly granular calorimeters
(Testbeams 2005 – 2009)



- 3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)
- Sizes : 380 380×200 mm3
- Thickness of slabs : 8.3 mm (W=1,4mm)
- VFE outside detector
- Number of channels : 9720 (10×10 mm²)
- Weight : ~ 200 Kg

Technological Prototype

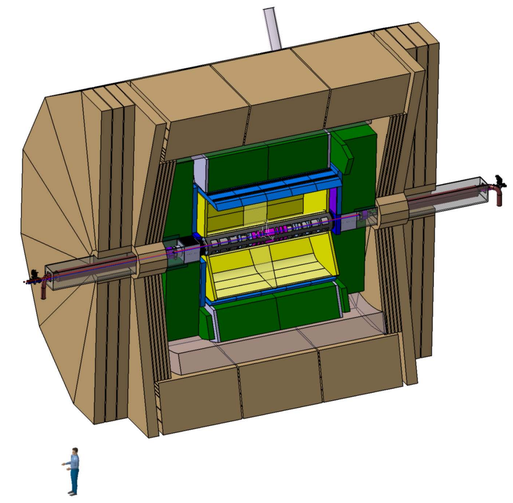
Addressing engineering Challenges
Confirming results of Physics Prototype
(Testbeams 2011 – 2014)



- 1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)
- Sizes : 1560 545×186 mm3
- Thickness of slabs : 6 mm (W=2,1mm)
- VFE inside detector
- Number of channels : 45360 (5×5 mm²)
- Weight : ~ 700 Kg

ILC Detector

Combining Physics and Technological Prototype

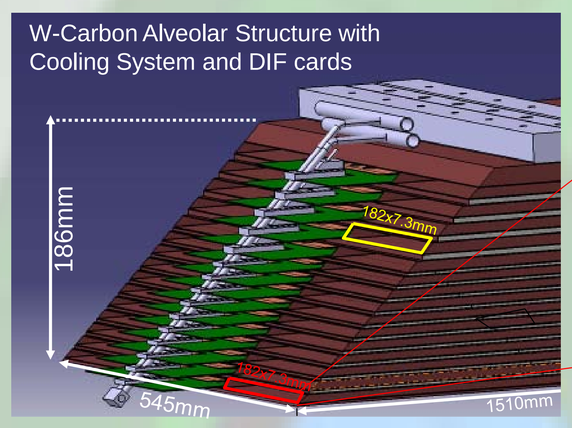


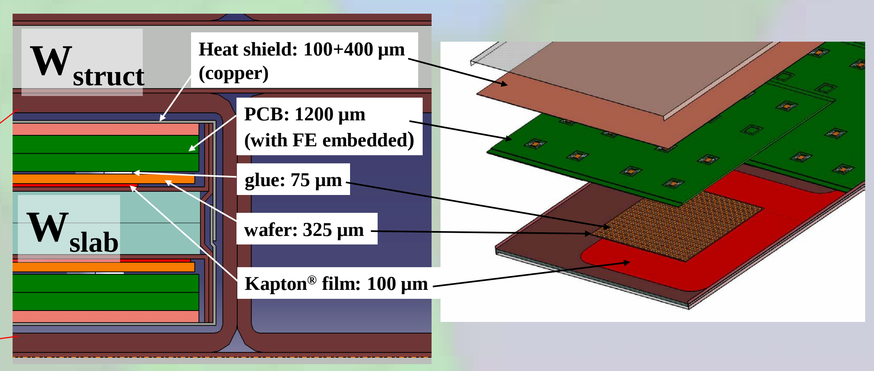
Electromagnetic Calorimeter :
- Cells : 110 10^6
- Total Weight : ~130 t

Design Guidelines:

As compact as possible
- Calorimeters to be placed inside magnetic coil

"4π" Hermetic
- Precision Physics at ILC requires full acceptance



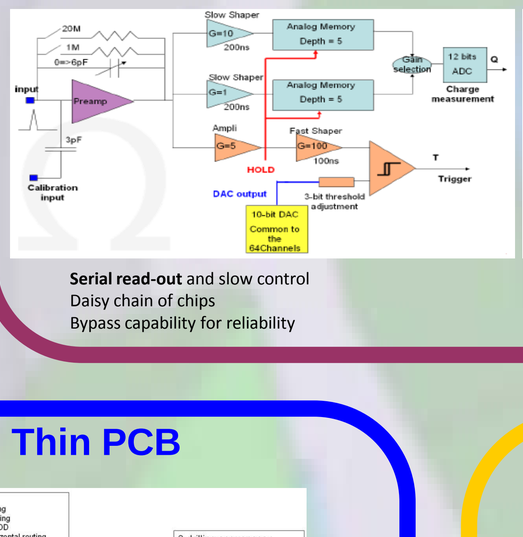


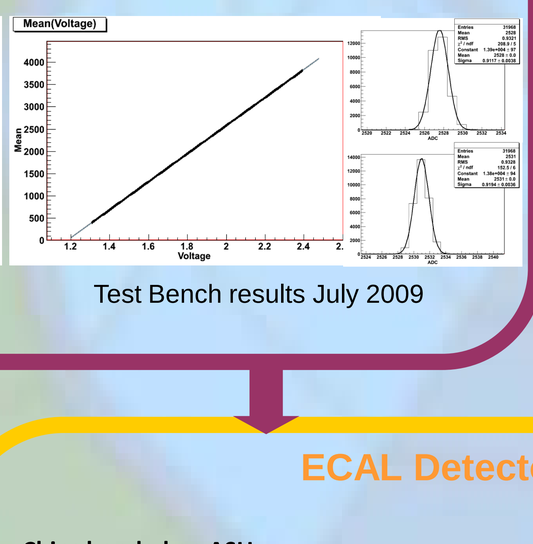
Silicon Kalorimeter Integrated Read Out Chip : SKIROC

SKIROC has 64 independent channels
- With **auto-trigger** feature
- Analogue shaping
- **Digitization : 12 bits**
- Storage
- No external components

Excellent S/N ratio
Targeting 10
Obtained 9 with cosmics And 7 on beam

15 bits resolution with 2 gains
DC coupled



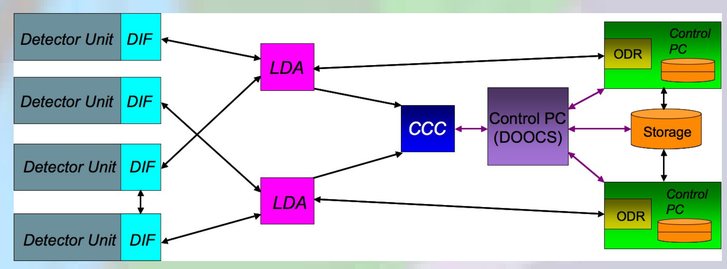


Serial read-out and slow control
Daisy chain of chips
Bypass capability for reliability

Test Bench results July 2009

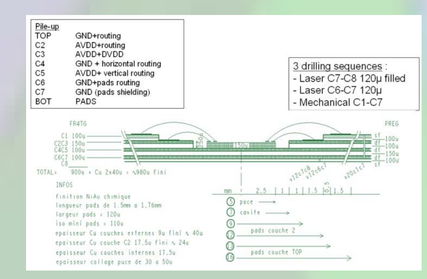
A generic DAQ System

Standard HDMI connectors, LVDS, GBEthernet, Optical links
Generic FPGA
Scalable

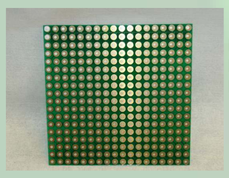


Detector Extremity - Detector Interface Card
Linked Data Aggregator
Clock, Commands and Control
Off Detector Receiver

Thin PCB



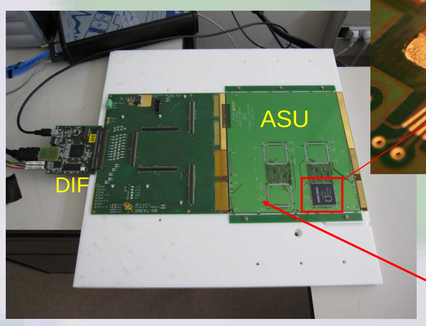
PCB to be glued onto Si Wafer
Epotek E-4110



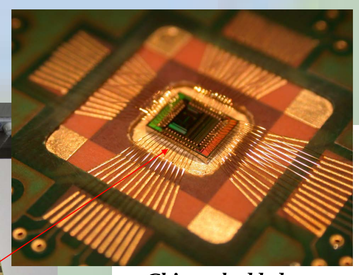
Typical Values:
Dot Thickness: 66 ⎧m
Dot Diameter: 3 mm
R_{Dot} < 0.005 Ω

ECAL Detector Slab

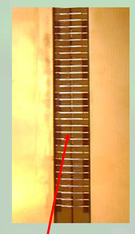
Chips bonded on ASU
(Active Sensor Units)
Unity of Chips, PCB and Si Wafers



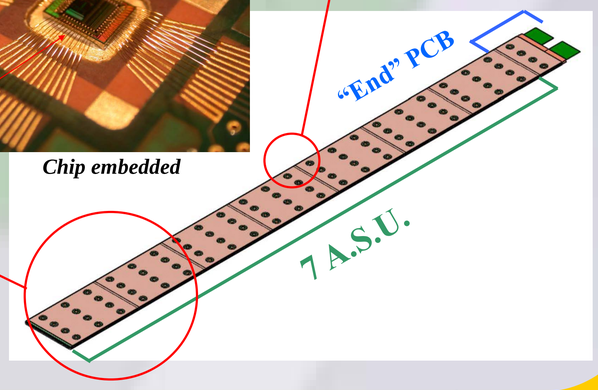
First ASU Prototype - July 2009



Chip embedded

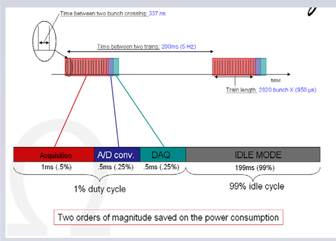


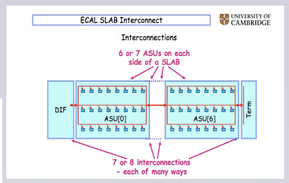
Flat Flexible Cable Connection between 2 A.S.U.



Signal Integrity & Power Supplies

Power pulsing with
3 kW/100 million channels
Scaled to EUDET : 700 W !
For the whole module





10 mF as local battery
For power storage
Support 1% duty cycle
Minimizing voltage drop

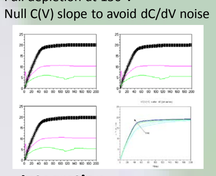
PIN Diodes Silicon Sensors

Design

Designed for ILC : **Low cost, 3000 m2**
Minimized number of manufacturing steps
Target is 2 EUR/cm2
Now : 15 EUR/cm2
Use of **floating guard-rings**

I(V) and C(V) characterization

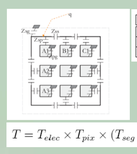
Breakdown voltage >500V
Current leakage <4 nA/pixel (chip is DC coupled)
Full depletion at 150 V
Null C(V) slope to avoid dC/dV noise



Integration

Glued on a PCB
Glue compatibility is studied
Automated procedure for glue deposition
256 glue dots, 75 µm thick, 3 mm diameter

EUDET layout
Prototype from Hamamatsu

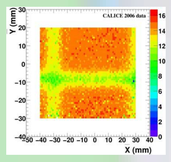


Pixel	Continuous	1 cm	3 mm
A1 (ref)	0	0	-14.5
A2	-6	-21.6	-75
A3	0	-34.6	-138

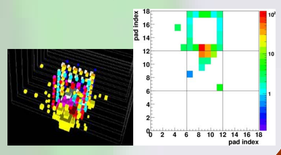
$$T = T_{elec} \times T_{pix} \times (T_{seg} \times T_{ss})^{N_{seg}} \times T_{seg} \times T_{inj}$$

Known issues

Dead space optimization
Guard-rings do not collect charges
Dead space to be reduced



Crosstalk due to floating guard-rings
Due to capacitive couplings
From metal layers at the surface

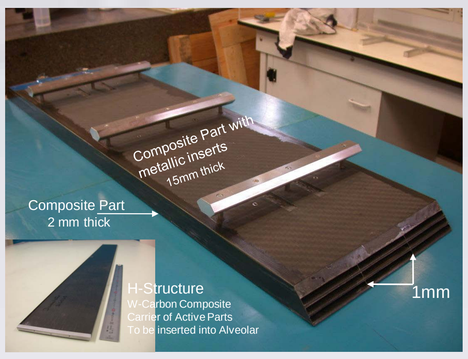


R&D on crosstalk

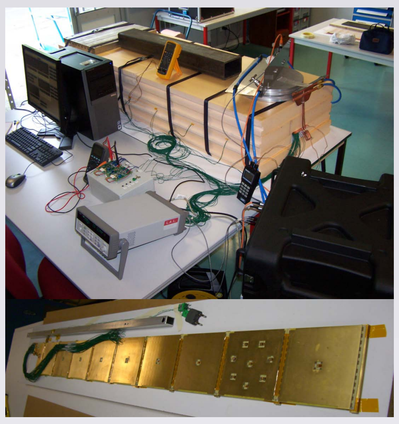
Segmented guard-rings layout
Simulation models at silicon or Electrical level

Demonstrator to validate mechanical concept

Alveolar Structure



Thermal tests to control power consumption



Thermal layer with 9 interconnected ASUs